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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,195	08/27/2003	Pachinco Yang	BHT-3212-38	3475

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,195	YANG, PACHINCO	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *27 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

1. Claims 1 – 14 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 11, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Broberg et al (US6601122) herein after Broberg.

4. As to claim 1, Broberg discloses a data processing system comprising: a set of memory modules for storing program instructions and data, the set of memory modules comprising at least one low-speed memory and at least one high-speed memory, the low-speed and high-speed memories both storing an vector table individually for recording at least one entry instruction of an service routine;

and a microprocessor comprising: a central processing unit (CPU) for executing program instructions and calculating data, wherein the CPU is designed to fetch the program instructions in the low-speed memory when an interruption occurs; (Broberg teaches of a data processing system as shown in figure 3, with memory modules

56,58,and 60, and including CPU on chip memory 110 of processing unit and processing unit 50 also comprising a processing unit. Said processing unit has CPU 50 that perform instruction transaction in block 122 of figure 4, COL. 6, lines 12 - 14) and a memory controller to enable the CPU, under the memory controller's control, to fetch the program instruction and access the data in the set of memory modules, the memory controller also comprising a re-addressing device; (Broberg teaches of instruction fetch unit 122 of figure 4 that has a re-addressing function that get instruction from on chip memory 110 or of chip memory 56)

wherein, when the interruption occurs, the CPU generates an interrupt vector address to the memory controller, and if the re-addressing device of the memory controller identifies that the address falls within the address range of the interrupt vector table, the re-addressing device sends out an enable signal to the high-speed memory to enable the CPU to fetch the corresponding entry instruction of the interrupt service routines in the high-speed memory, instead of the predetermined low-speed memory, so as to reduce the interrupt latency when fetching the program instruction. (Broberg teaches of CPU generating an interrupt vector address, (COL. 2, lines 30 – 34). Broberg teaches of an override address register 112 that comprises the re-address table that creates enable signal 114 of figure 4. This enables the interrupt routine comprising 110 to be used instead of the non-critical version, COL. 6, lines 47 – 62).

5. As to claim 2, Broberg discloses the data processing system of claim 1, wherein the re-addressing device comprises: a first address decoder for decoding an original

address generated by the CPU to identify whether the original address falls within the address range of the interrupt vector table, and to generate a corresponding identifying signal; (Broberg teaches of default address 118, and override address 120. It is inherent that a first address decoder would be present to create validation signal 114 to choose which ISR will be chosen)

a multiplexer for selecting between the original address generated by the CPU and a predetermined re-directing address as a valid address according to the identifying signal; and a second address decoder for decoding the valid address generated by the multiplexer to determine whether the enable signal is sent to the high-speed memory or the low-speed memory. (Broberg teaches of said multiplexer in 116 of figure 4, Col. 6, lines 52 – 54).

6. As to claim 3, Broberg discloses the data processing system of claim 2, wherein the re-directing address is programmable, and falls within the address range of the high-speed memory, distinguishably from the vector addresses of the low-speed memory. (Broberg teaches that said address is programmable, as it comprises a look up table, and is distinguishable from low speed memory 118 of figure 4).

7. As to claim 4, Broberg discloses the data processing system of claim 1, wherein the microprocessor further comprises an on-chip high-speed memory, and the on-chip high-speed memory also comprises an interrupt vector table for recording at least one entry instruction of the interrupt service routines, and the vector address range is the

same as the vector address range of the interrupt vector table of the low-speed memory. (Broberg claims said memory features with the vector table, 120, and on chip memory 110 of figure 4).

8. As to claim 5, Broberg discloses the data processing system of claim 4, wherein the re-addressing device comprises: a first address decoder for decoding an original address generated by the CPU to determine whether the original address falls within the address range of the interrupt vector table, and to generate a corresponding on-chip enable signal to enable the on-chip high-speed memory; a second address decoder for decoding the original address generated by the CPU to determine whether the original address falls within the address range of the high-speed or the low-speed memory, and correspondingly to generate a high-speed enable signal to enable the high-speed memory, or to generate an identifying signal of the low-speed memory ;(Broberg teaches of a special register 113 being written with the appropriate address of the interrupt routine, implying the inherent presence of said decoder, COL. 6, lines 47 – 49)

and an XOR gate for receiving the on-chip enable signal and the identifying signal of the low-speed memory to perform exclusive-or operation, and correspondingly to generate a low-speed enable signal to enable the low-speed memory. (Broberg teaches in figure 4 with mux, 116 that inherently comprises said XOR gate to create said enabling signal, COL. 6, lines 52 – 56).

9. As to claim 6, Broberg discloses the data processing system of claim 1, wherein the low-speed memory is a non-volatile memory. (Broberg teaches in figure 3 of said memory (60) being non-volatile, COL. 4, lines 47 – 50).

10. As to claims 7 and 8, Broberg discloses the data processing system of claim 6, wherein the non-volatile memory is an electrical programmable read-only memory (EPROM). (Broberg teaches such memory being EPROM, or FLASH, COL. 4, lines 55).

11. As to claims 9 and 11, Broberg discloses the data processing system of claim 1, wherein the high-speed memory is a volatile memory. (Broberg teaches that said memory is a volatile memory, COL. 6, lines 25 – 29).

12. As to claim 10, Broberg discloses the volatile memory is an external dynamic random access memory (DRAM) built outside the microprocessor. (Broberg teaches in figure 2 that external memory is a RAM 56. It would have been inherent to use a fast DRAM to support this reduced latency scheme should microprocessor does not comprise an on-chip memory).

13. As to claim 13, Broberg discloses the data processing system of claim 1, wherein the data processing system further comprises a power source for providing electrical power to the data processing system, and when the power source is shut

down, the program instructions and data stored in the high-speed memory are lost; however the program instructions and data stored in the low-speed memory are preserved. (Broberg teaches in figure 3 of a system using a battery-pack CMOS RAM that would preserve data when electrical power is removed, COL. 4, lines 52 – 57).

14. As to claim 14, Broberg discloses the data processing system of claim 1, wherein the data processing system further comprises a bus connected to the CPU, the memory controller, and the set of memory modules for transmitting the program instructions and data. (Broberg teaches in figure 3 of system bus 5, connecting said elements to enable computing transactions, COL. 4, lines 37 – 46).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Broberg in view of Godfrey (US6889279).

As to claim 12, Broberg does not disclose a non-PC architecture microprocessor. (However Godfrey teaches of an ARM processor that is non-PC, figure 3. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Broberg into Godfrey to provide a means of reducing interrupt intervals, COL. 1, lines 21 – 29).

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
5/27/2005

TIM VO
PRIMARY EXAMINER